URN etd-0407109-183705-293
Author Chen-Chia Yang
Author's Email Address No Public.
Statistics This thesis had been viewed 60 times. Download 0 times.
Department
Year 2006
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title A 64 Bit Asynchronous Low Power Consumption Comparator
Date of Defense 0000-00-00
Page Count 61

Keyword
Asynchronous
Comparator
Low Power
Expandability
Robustness

Abstract
In this paper, we propose a 64-bit low power asynchronous comparator which has flexibility, high expandability, and robustness. It is an asynchronous serial structural design. When compared result is equal, this computing result can be transmitted in next step by high bit to low bit. If compared result is not equal, the circuit will be stop and save unnecessary power consumption. Our design was implemented by using the process of TSMC's 0.35μm. The layout for the design was generated with SpringSoft Laker and verified by Mentor Calibre (for DRC and LVS checks). Since results show that its average power consumption and timing delay are 0.0166mW/MHz and 1.97ns, respectively, so our design can achieve a good performance.
Advisory Committee Jung-Lin Yang - advisor

Files No Any Full Text File.
Date of Submission 2007-08-17